

SEP 01



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Dinh, Son

Patent No.: 7,068,544

Group Art Unit: 2824

Issue Date: June 27, 2006

Docket No: 1303.014US1

Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
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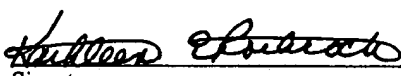
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PATENT NO : 7,068,544

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DATED : June 27, 2006

INVENTOR(S) : Forbes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 1, line 20, after "Insulators," insert - - attorney docket no. (Micron 01-0485), - -.

In column 2, line 55, delete "DEVICES" and insert - - DEVICES - -, therefor.

In column 4, line 6, delete "an" and insert - - a - -, therefor.

In column 4, line 36, delete "horizonal" and insert - - horizontal - -, therefor.

In column 5, line 58, delete "transistors," and insert - - transistors", - -, therefor.

In column 7, line 38, delete "adresses" and insert - - addresses - -, therefor.

In column 19, line 58, in Claim 24, delete "integrate" and insert - - intergate - -, therefor.

In column 22, line 26, in Claim 43, delete "fanned" and insert - - formed - -, therefor.

MAILING ADDRESS OF SENDER:

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Minneapolis, MN 55402

Atty Docket No: 1303.014US1

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